ANALOG DEVICES

AN-349
APPLICATION NOTE

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Keys to Longer Life for CMOS

Here's How CMOS Can Be Protected Against Abuses

by Jerry Whitmore

The two principal dangers to analog CMOS (Complementary-symmetry Metal-Oxide Semiconductors) are static electricity and overvoltage (signal voltages exceeding the supply). Both can be effectively dealt with by the aware user.

STATIC ELECTRICITY

The danger from electrostatic voltage buildup is that of "punch-through" of the thin oxide (or nitride) layer that insulates the gate from the substrate, due to accumulation of static charge ($V = q/C = 1kV/nC/pF$). This danger is minimal in working circuits, because the gate is protected by zener diodes on the chip, which permit depletion of the charge at safe levels. However, during socket insertion, it is possible for a large static charge to exist between the CMOS device and the socket. If the first pin plugged into the socket happens not to be common to the zener-diode protection circuit, the charge on the gate will discharge through the oxide layer, destroying the device. These four steps will help the device survive the system assembly stage.

1. Keep unused CMOS devices in the black conductive foam in which they were shipped to prevent charge buildup between pins.

2. Ground the operator, who is inserting the devices, to the system power ground with a plastic ground strap.

3. Before pulling the CMOS device from the protective foam, ground the foam to power common to deplete accumulated charge.

4. After the circuit has been inserted into a circuit board, keep the board grounded or shielded when carrying it around.

THE SCR "LATCH"

When working with analog CMOS circuits, the safest practice is to make sure that no analog or digital voltage applied to the device exceeds the supply voltage, and that the supply voltage itself is within ratings. Nevertheless, occasions do arise where it is necessary to tolerate overvoltage. Protection is possible in most cases, if the mechanism of failure is understood.

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Figure 1 shows the circuit and cross-section of a typical CMOS output switching element. From the connections and associations of the various elements and regions, we can draw an equivalent diode circuit (Figure 2). If the analog input voltage at either the S or the D terminals exceeds the power-supply

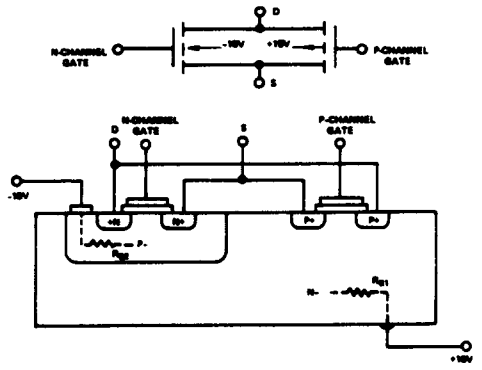


Figure 1. Cross-section of CMOS switching element

voltages, the parasitic transistors formed by the various diode junctions are placed in the forward bias mode. These parasitic NPN and PNP transistors appear to form the SCR ("silicon controlled-rectifier") circuit shown in Figure 3. Overvoltage

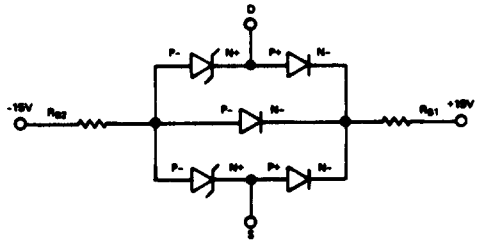
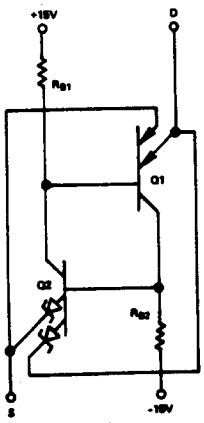


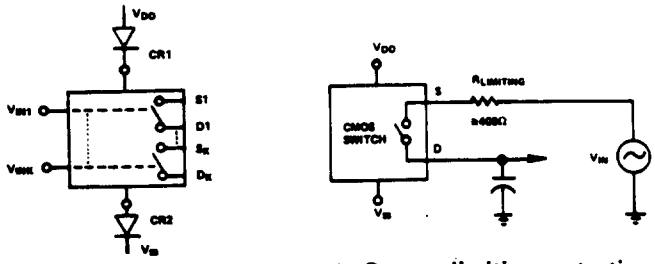
Figure 2. Diode equivalent circuit of CMOS switching element

can cause excessive current and metallization failure. Normally, the outputs of op amps are used as the voltage sources feeding the S or D terminals, so the currents cannot exceed the op amps' dc output current limitations. Nevertheless, it is still possible for transient induced currents to destroy the CMOS device; protection is therefore desirable.



IF, FOR EXAMPLE, A POSITIVE OVER-VOLTAGE IS APPLIED TO THE DRAIN TERMINAL, THE BASE OF Q1 WILL CONDUCT WHEN ITS EMITTER VOLTAGE EXCEEDS V_{DD} BY ONE BASE-EMITTER DROP. THE COLLECTOR CURRENT WILL INCREASE TO A LEVEL LIMITED ONLY BY THE V_{SS} AND V_D CURRENT LIMITATIONS. SINCE THE METAL INTERCONNECT TO THE SUPPLY TERMINAL IS NORMALLY DESIGNED TO HANDLE SMALL CURRENTS, THE CURRENT DENSITIES INVOLVED CAN CAUSE DEVICE FAILURE.

Figure 3. Parasitic transistor action in CMOS switch



a. Diode protection

b. Current-limiting protection

Figure 4. Circuit protection schemes

Figure 4 illustrates a means of preventing turn-on of the parasitic transistors by means of diodes (say 1N459's) in series with the supply leads. If the S or D terminal is at a higher-than-supply voltage, CR1 and/or CR2 are reverse-biased and base drive is unavailable to turn the transistors on. A separate pair of diodes should be used for each CMOS device to be protected. Though powerful, the method is not infallible. If one terminal of the switch is tied to a negative potential (e.g., a charged capacitor), and the other terminal is raised above V_{DD}, the avalanche diode at one emitter of Q2 is sufficient to supply enough base drive to turn Q2 on, despite the protective diodes. For such a situation, a current-limited supply, or resistance in series with the capacitor is necessary.

If transient overvoltages are expected at the S or D terminals, 300–400Ω in series with the terminal to be fed by the voltage source is suggested (Figure 4b).